ELE 448 Lab 4

Due by 04 March, 2020

Introduction:

This week in lab, we will be creating a schematic, simulation, and layout for a XOR, static negative level D-latch, static positive level D-latch, and static positive level D-latch with a reset. To reduce the workload of the lab, templates are provided for the layouts. In order to add these templates to your directory, please follow the following steps:

1. Open the command terminal on a linux machine
2. Type:
   cp -a /u/ugrads/tmauldin/Public/Templates/ /u/ugrads/<your_username>/<your_directory_name>/
   a. Don't include "<>" in the path
3. Start Cadence (IC615)
4. Create a new library with the following properties
   - Name: Templates
     - The name is case sensitive
   - Path: /u/ugrads/<your_directory_name>
   - Attach to TSMC 0.2u CMOS018

In the library you will see three layouts

- dlatchTemp0_180 (use for NL/PL D-latches)
- dlatchTemp1_180 (use for PL D-latch with reset)
- Xor2Temp0_180 (use for XOR)

In the template for the latches, you will notice some metal rails in the bottom of the layouts. These are used for signals that have to be distributed throughout the layout, such as the clock. Be sure to utilize them in your layout.

When you are running simulations, be sure to show every possible situation. This will allow you to fully validate the function of a given component. In addition, ensure that you give appropriate names to the nets of interest so it is clear which signals are being viewed in the ADE.

Instructions:

The tasks listed below apply to the XOR, PL D-Latch, NL D-Latch, and the PL D-Latch with Reset.

1. Create a schematic
2. Create a symbol
3. Run a simulation and verify its functionality
4. Create a layout

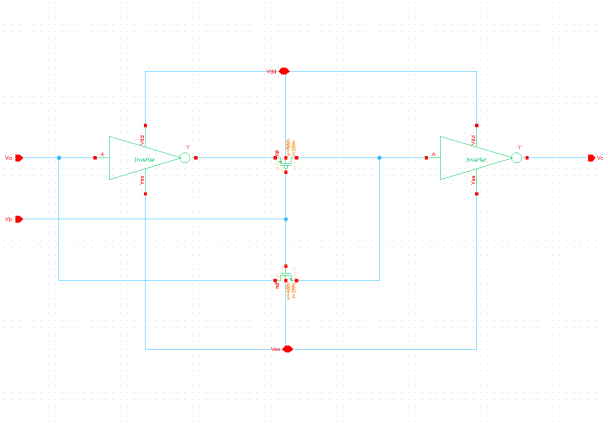

Figure 1 - XOR

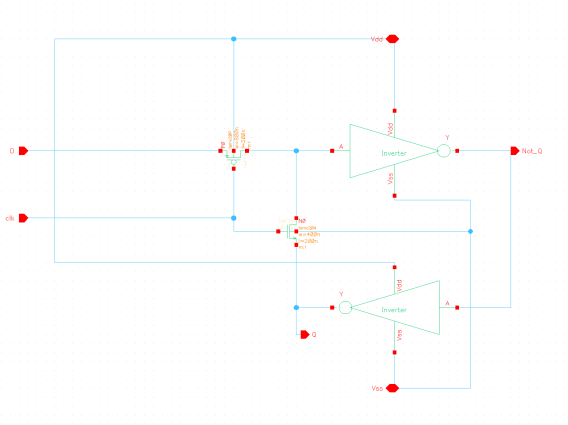

Figure 2 - Negative Level D-Latch

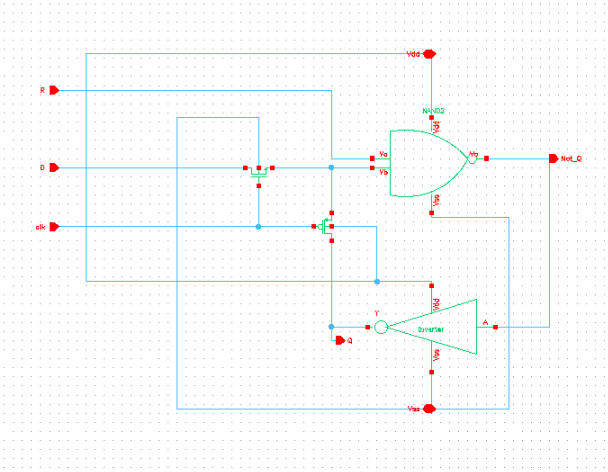

Figure 3 - Positive Level D-Latch with a Reset

Lab Write-up:

For all components:

a. Schematic
   i. Provide an image
   ii. How many of each type of MOSFET were used in your design?
   iii. How does the component work?
b. Simulation
   i. Provide images
      1. Simulation setup and results
   ii. Does the output make sense?
      1. Provide a truth table
c. Layout
   i. Show an image of your layout
   ii. Explain how the device is represented in the layout
      1. Where is each component located?
   iii. Did DRC and LVS pass?
      1. If it failed, what did you have to modify to get them to pass?